UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,611	06/03/2005	Masaru Kuramoto	Q88048	4984

23373 7590 04/03/2009
SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
KIM, JAY C	

ART UNIT	PAPER NUMBER
2815	

MAIL DATE	DELIVERY MODE
04/03/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/537,611	KURAMOTO ET AL.	
	Examiner	Art Unit	
	JAY C. KIM	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed March 16, 2009.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tadatomo et al. (US 6,225,650) in view of Motoki et al. (US 2003/0145783).

Regarding claim 1, Tadatomo et al. disclose a nitride semiconductor substrate (Fig. 4) comprising a group III nitride semiconductor substrate (3) (col. 5, lines 25-26), a mask (21) (col. 5, lines 27-28) formed over the group III nitride semiconductor substrate (3), and a group III nitride semiconductor multilayer film (31) or a film of multilayer GaN (col. 5, line 30) formed above the mask (21).

Tadatomo et al. differ from the claimed invention by not showing that the group III nitride semiconductor substrate has a dislocation density in a vicinity of a surface thereof of $1 \times 10^7/cm^2$ or less, and the mask has a polycrystalline material deposited on a surface thereof.

Motoki et al. disclose a group III nitride semiconductor substrate (Fig. 10(5)) formed by GaN single crystal growth (Fig. 10(4)), which has a dislocation density in a vicinity of a surface thereof less than $1 \times 10^7/cm^2$ (lines 7-8 of [0316]). Motoki et al.

further disclose a nitride semiconductor substrate (Fig. 5), wherein a mask (23) (SiO_2 on line 1 of [0183]) may have a polycrystalline material (polycrystalline GaN, line 2 of [0183]) deposited on a surface thereof.

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate grown by HVPE (hydride vapor phase epitaxy), it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the nitride semiconductor substrate disclosed by Tadatomo et al. may have a low dislocation density and the mask disclosed by Tadatomo et al. may have a polycrystalline material deposited on a surface thereof as disclosed by Motoki et al., because the combined nitride semiconductor substrate could be used for improving device characteristics due to low dislocation density of the substrate, and a multilayer mask structure for GaN crystal growth is well-known and the polycrystalline material could be used for improving GaN growth. Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

Regarding claim 2, Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that the polycrystalline material is formed from a material containing aluminum and nitrogen as essential elements.

Motoki et al. further disclose that the mask (23) may be made of polycrystalline aluminum nitride (AlN) or polycrystalline gallium nitride (GaN) ([0182]).

Since Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to replace the polycrystalline GaN deposited on the mask disclosed by Tadatomo et al. in

view of Motoki et al. with the polycrystalline AlN disclosed by Motoki et al., because both polycrystalline AlN and polycrystalline GaN may be used to grow high quality single crystal GaN. Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

Regarding claim 3, Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that voids are formed on the surface of the mask having the polycrystalline material.

Motoki et al. further disclose that voids (voluminous defects in voluminous defect accumulating region H in Fig. 5(a)(3)) are formed on the surface of the mask (23) having the polycrystalline material (lines 7-9 of [0299], lines 1-3 of [0420], and lines 11-13 of [0427]).

Since Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the nitride semiconductor substrate disclosed by Tadatomo et al. in view of Motoki et al. may comprise voids formed on the surface of the mask having the polycrystalline material as disclosed by Motoki et al., because voids would be formed on a mask while growing single crystal GaN due to imperfect growth of single crystal GaN on an amorphous or polycrystalline material.

Regarding claim 4, Tadatomo et al. further disclose for the nitride semiconductor substrate according to Claim 1 that the mask (21) is provided on a surface of the group III nitride semiconductor substrate (3).

Regarding claim 6, Tadatomo et al. disclose a nitride semiconductor device (semiconductor light emitting element formed on substrate shown in Fig. 4) (col. 1, lines 7-9) comprising a group III nitride semiconductor substrate (3) (col. 5, lines 25-26), a mask (21) (col. 5, lines 27-28) formed over the group III nitride semiconductor substrate (3), and a group III nitride semiconductor multilayer film (col. 5, lines 16-21) formed above the mask (21), the group III nitride semiconductor multilayer film including an active layer.

Tadatomo et al. differ from the claimed invention by not showing that the group III nitride semiconductor substrate has a dislocation density in a vicinity of a surface thereof of $1 \times 10^7/cm^2$ or less, and the mask has a polycrystalline material deposited on a surface thereof.

Motoki et al. disclose a group III nitride semiconductor substrate (Fig. 10(5)) formed by GaN single crystal growth (Fig. 10(4)), which has a dislocation density in a vicinity of a surface thereof less than $1 \times 10^7/cm^2$ (lines 7-8 of [0316]). Motoki et al. further disclose a nitride semiconductor substrate (Fig. 5), wherein a mask (23) (SiO_2 on line 1 of [0183]) may have a polycrystalline material (polycrystalline GaN on line 2 of [0183]) deposited on a surface thereof.

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate grown by HVPE (hydride vapor phase epitaxy), it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the nitride semiconductor device disclosed by Tadatomo et al. may comprise a low dislocation density group III nitride semiconductor substrate and a mask having a polycrystalline material deposited on a surface thereof as disclosed by Motoki et al., because the

combined nitride semiconductor device would have improved device characteristics due to low dislocation density of the substrate, and a multilayer mask structure for GaN crystal growth is well-known and the polycrystalline material could be used for improving GaN growth. Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

Regarding claim 7, Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that the polycrystalline material is formed from a material containing aluminum and nitrogen as essential elements.

Motoki et al. further disclose that the mask (23) may be made of polycrystalline aluminum nitride (AlN) or polycrystalline gallium nitride (GaN) ([0182]).

Since Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to replace the polycrystalline GaN deposited on the mask disclosed by Tadatomo et al. in view of Motoki et al. with the polycrystalline AlN disclosed by Motoki et al., because both polycrystalline AlN and polycrystalline GaN may be used to grow high quality single crystal GaN. Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

Regarding claim 8, Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that voids are formed on the surface of the mask having the polycrystalline material.

Motoki et al. further disclose that voids (voluminous defects in voluminous defect accumulating region H in Fig. 5(a)(3)) are formed on the surface of the mask (23) having the polycrystalline material (lines 7-9 of [0299], lines 1-3 of [0420], and lines 11-13 of [0427]).

Since Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the nitride semiconductor device disclosed by Tadatomo et al. in view of Motoki et al. may comprise voids formed on the surface of the mask having the polycrystalline material as disclosed by Motoki et al., because voids would be formed on a mask while growing single crystal GaN due to imperfect growth of single crystal GaN on an amorphous or polycrystalline material.

Regarding claim 9, Tadatomo et al. further disclose for the nitride semiconductor device according to Claim 6 that the mask (21) is provided on a surface of the group III nitride semiconductor substrate (3).

Regarding claim 11, Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that the mask is provided in a vicinity of a device separating groove of the nitride semiconductor device.

Tadatomo et al. further disclose that a mask (2 in Fig. 11) is provided in a vicinity of a device separating groove (groove separating the devices in Fig. 11) (col. 10, lines 24-26) of the nitride semiconductor device (Fig. 11).

Since Tadatomo et al. teach a nitride semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor device disclosed by Tadatomo et al. in view of

Motoki et al. with the device separating groove disclosed by Tadatomo et al., because forming a stripe laser comprising a device separating groove is well-known in manufacturing a nitride semiconductor device as well as forming an individual nitride semiconductor device shown in Fig. 9(b) of Tadatomo et al.

Response to Arguments

3. Applicants' arguments filed March 16, 2009 have been fully considered but they are not persuasive.

Applicants argue that "the Examiner's proposed combination, namely, that "the nitride semiconductor substrate disclosed by Tadatomo et al may have a low dislocation density and the mask disclosed by Tadatomo et al may have a polycrystalline material deposited on a surface thereof as disclosed by Motoki et al" is based on improper hindsight". In response to applicants' argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Applicants argue that "if the nitride semiconductor substrate disclosed by Tadatomo et al had a low dislocation density as disclosed by Motoki et al, as suggested by the Examiner, many dislocations would develop from the vicinity of the mask". As

stated in rejection of claims 1 and 6, Tadatomo et al. in view of Motoki et al. disclose all the limitations recited in claims 1 and 6. Therefore, it is not clear whether Applicants argue that "many dislocations would develop from the vicinity of the mask" in the claimed inventions.

Applicants argue that "that is, Tadamoto [sic] et al already teaches that a *GaN group crystal base member almost without dislocations* can be obtained", and that "therefore, one skilled in the art would not have been motivated to employ a nitride semiconductor substrate having a low dislocation density in the device of Tadatomo et al, where more dislocations would be generated". Tadatomo et al. clearly disclose a dislocation density in a GaN substrate (3), and extension of the dislocation line shut off in a GaN film (31). That is, the mask (21) shown in Fig. 4 of Tadatomo et al. would reduce a dislocation density in the GaN film (31) in contrast to Applicants' argument.

Applicants argue that "since the mechanism of dislocation generation in the above cases is different from that in the case where a Group III nitride crystal is grown on a substrate of a Group III nitride, it is not clear from the disclosure of Motoki et al that the polycrystalline material on the mask film has effects on the dislocation density, in the case where a Group III nitride crystal is grown on a substrate of a Group III nitride". Motoki et al. clearly disclose a GaN substrate ([0192]), and growing a GaN film on a GaN substrate using a mask coated with a polycrystalline material ([0184]), which would have a similar structure shown in Fig. 4 of Tadatomo et al. Further, Applicants do not provide any evidence that a mask coated with a polycrystalline material cannot be used in Tadatomo et al. in view of Motoki et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the

intended use. *In re Leshin*, 125 USPQ 416. Still further, it is not necessary that the prior art suggest the combination to achieve the same advantage or result discovered by applicant. See MPEP 2144.

Applicants argue that "accordingly, one skilled in the art would not have been motivated to apply the mask with polycrystalline material on the surface thereof to the nitride semiconductor substrate disclosed by Tadatomo et al having a low dislocation density, as proposed by the Examiner, since Motoki et al does not teach or suggest that the polycrystalline material could be used for improving GaN growth". See the above responses.

Conclusion

4. Applicants' amendment necessitated the new ground of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571)270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Examiner, Art Unit 2815
March 31, 2009

/Jerome Jackson Jr./
Primary Examiner, Art Unit 2815